REMARKS

An Office Action was mailed on December 27, 2002. Claims 1 – 53 are pending in the present application. Claims 47 and 48 are amended No new matter is introduced.

OBJECTION TO CLAIMS

Claims 47 and 48 are objected to for certain informalities. Applicants amend claims 47 and 48 to correct these informalities, and respectfully request that the objections be withdrawn.

OBJECTION TO DRAWING, SPECIFICATION

The specification and drawing are objected to for failing to illustrate and describe FIGs. 8A and 8B, which the Examiner suggests are introduced at page 19, line 8 of Applicants' specification. In fact, the references at page 19, line 8 are made to reference numerals 8A, 8B depicting interleaving/de-interleaving apparatuses as illustrated in Applicants' FIG. 4 and described in surrounding text in the specification (see, e.g., page 18, line 16 – page 18, line 25 of Applicants' specification). Applicants respectfully submit that interleaving/de-interleaving apparatuses 8A, 8B are adequately depicted in FIG. 4 and described in the specification, and request that these objections be withdrawn.

REJECTIONS UNDER 35 U.S.C. § 112

Claims 1 – 53 are rejected under the first and second paragraphs of 35 U.S.C. § 112 for "failing to describe in the specification how to manipulate data in a single matrix by simultaneously interchanging rows and columns using said single matrix without losing track of the location of said original data".

Applicants claimed interleaving method and apparatus operates by first interchanging rows of the matrix according, and then by interchanging columns of the matrix according to a predetermined order (effectively in a sequential rather than simultaneous manner). Circuitry for performing interleaving is described, for example, in Applicants' specification at page 23, line 13 through page 34, line 8 and with reference to FIGs. 10 and 11. Circuitry for performing de-interleaving is described, for example, page 40, line 14 through page 43, line 6 and with reference to FIG. 14. Alternate embodiments of the interleaving/de-interleaving circuits are described in Applicants' specification following the descriptions for FIGs. 10, 11 and 14. Typically, interchange steps are accomplished by manipulating associated cell addresses in a physical memory rather than by rearranging the cell data in memory.

Applicants submit that the above-referenced descriptions adequately describe how matrix data is manipulated and tracked for performing interleaving and de-interleaving operations, and therefore respectfully request that the current rejections under 35 U.S.C. § 112 be withdrawn.

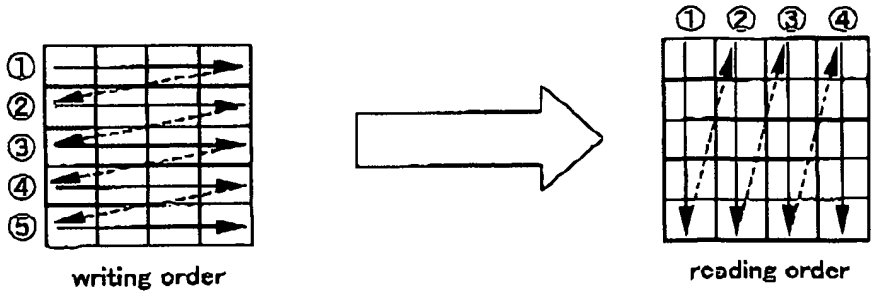
REJECTIONS UNDER 35 U.S.C. § 103

Claims 1 – 53 under 35 U.S.C. § 103(a) are rejected as being unpatentable over Applicants' admitted prior art (AAPA) in view of U.S. Patent No. 5.068,878 to Lin et al. Claims 1, 2, 3, 10, 17 – 24, 31 – 32, 35 – 36, 43, 46 and 49 are rejected under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view of U.S. Patent No. 4,959,863 to Azuma et al., as being unpatentable over AAPA in view of "Turbo Code ..." to Yamaguchi et al., and as being unpatentable over AAPA in view of U.S. Patent No. 5,204,981 to Karasawa et al. Claims 1, 2, 3, 10, 18 – 20, 23 – 24, 31- 32, 35 – 36, 43, 46 and 49 are rejected

under 35 U.S.C. § 103(a) as being unpatentable over Karasawa in view of Yamaguchi and "Two-Dimensional Interleaving ..." to de Almeida et al., and as being unpatentable over Karasawa in view of Azuma and de Almeida. Applicants respectfully traverse these rejections.

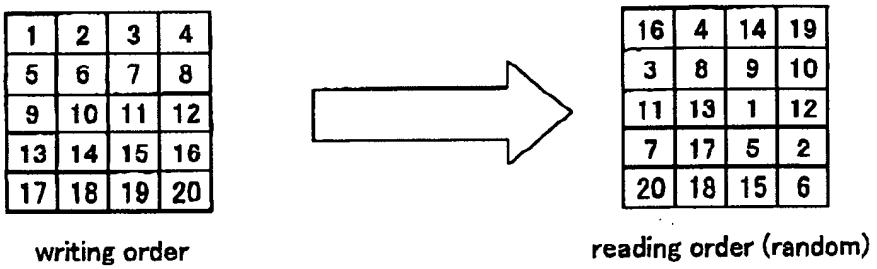
In independent claims 1 – 3, 10, 17 – 20, 23, 24, 31, 32, 35, 36, 43, 46 and 49, Applicants disclose a method and apparatus interleaving and de-interleaving data, whereby the data is rearranged by interchanging rows of the matrix according to a predetermined order, and then by interchanging columns of the matrix according to a predetermined order. Thus, in this described two-step process, the required units of interleaving are whole rows and whole columns. By first interleaving whole rows and then interleaving whole columns, data may be effectively randomized for transmission, for example, to avoid a severe impact associated with burst errors. At the same time, the complexity and cost of interleaving circuitry and algorithms is substantially reduced over conventional interleaving/de-interleaving methods.

AAPA describes several conventional interleaving/de-interleaving methods. For example, as described with reference to Applicants' FIG. 22, one prior art method simply writes data to a matrix in row order and reads the data in column order:



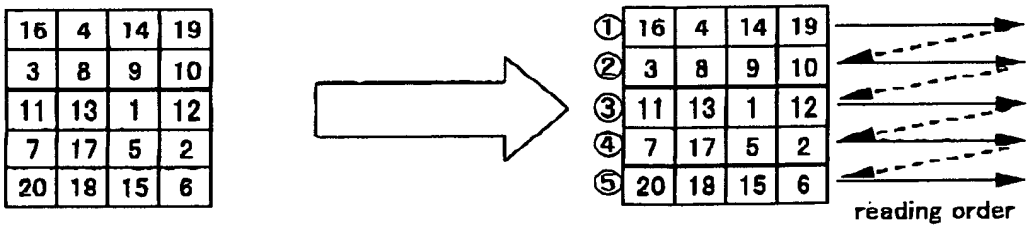
(Corresponds to FIG.22 of Prior Art)

As described with reference to Applicants' FIG. 23, another prior art method randomly reorders cell data in the matrix, and randomly the re-ordered data:



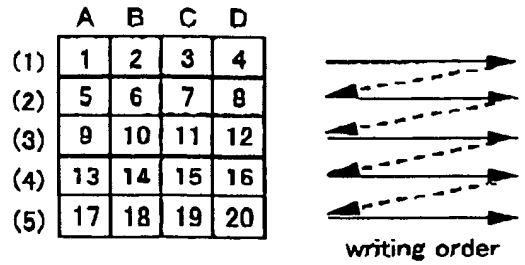
(Corresponds to FIG.23 of Prior Art)

A third prior art method described with reference to Applicants' FIG. 24 randomly writes data to cells of the matrix and reads data in row order:



(Corresponds to FIG.24 of Prior Art)

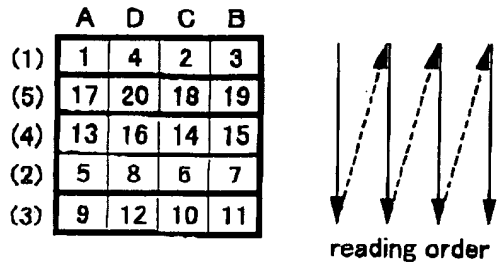
In Applicants' interleaving method as disclosed for example in FIG. 6, data is first written in row order to the matrix:



Next, as shown for example in Applicants' FIG. 7, row data is interchanged in the matrix without changing the order of cell data in each row:

	A	D	C	B
(1)	1	4	2	3
(2)	5	8	6	7
(3)	9	12	10	11
(4)	13	16	14	15
(5)	17	20	18	19

Then, as illustrated for example in Applicants' FIGs. 8 and 9, column data is interchanged in the matrix without changing the order of cell data in each column, and data is read from the matrix in column order:



Unlike Applicants claimed apparatus and method, none of AAPA and the cited references suggest or otherwise disclose a method of interleaving/de-interleaving in

which rows of a matrix are first reordered without changing the order of cell data in each row, and columns are then reordered without changing the order of cell data in each column, in order to produce cell data that has been effectively randomized in the matrix. Applicants' claimed method provides the strong advantage of providing for rearranged cell data that is highly resistant to burst errors in a manner that can be implemented by relatively simple circuits and algorithms. As a result, Applicants respectfully submit that independent claims 1 – 3, 10, 17 – 20, 23, 24, 31, 32, 35, 36, 43, 46 and 49 are allowable. As claims 4 – 9, 11 – 15, 21, 22, 25 – 30, 33, 34, 37 – 42, 44, 45, 47, 48 and 50 – 53 each depend from one of allowable claims 1 – 3, 10, 17 – 20, 23, 24, 31, 32, 35, 36, 43, 46 and 49, Applicants further submit that claims 4 – 9, 11 – 15, 21, 22, 25 – 30, 33, 34, 37 – 42, 44, 45, 47, 48 and 50 – 53 are allowable for at least this reason.

CONCLUSION

An earnest effort has been made to be fully responsive to the Examiner's objections. In view of the above amendments and remarks, it is believed that independent claims 1 – 3, 10, 17 – 20, 23, 24, 31, 32, 35, 36, 43, 46 and 49, and the claims that depend therefrom, stand in condition for allowance. Passage of this case to allowance is earnestly solicited. However, if for any reason the Examiner should consider this application not to be in condition for allowance, he is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fees due with this paper may be charged on Deposit Account 50-1290.

Respectfully submitted,

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